AndesCore™ N22, RISC-V Ultra-Compact Processor Solution

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2019 RISC-V CON

Agenda

- AndesCore™ N22, RISC-V Ultra-Compact Processor
- Supporting Infrastructure
  - Handy Pre-integrated Platform
  - Comprehensive Development Environment
- Summary

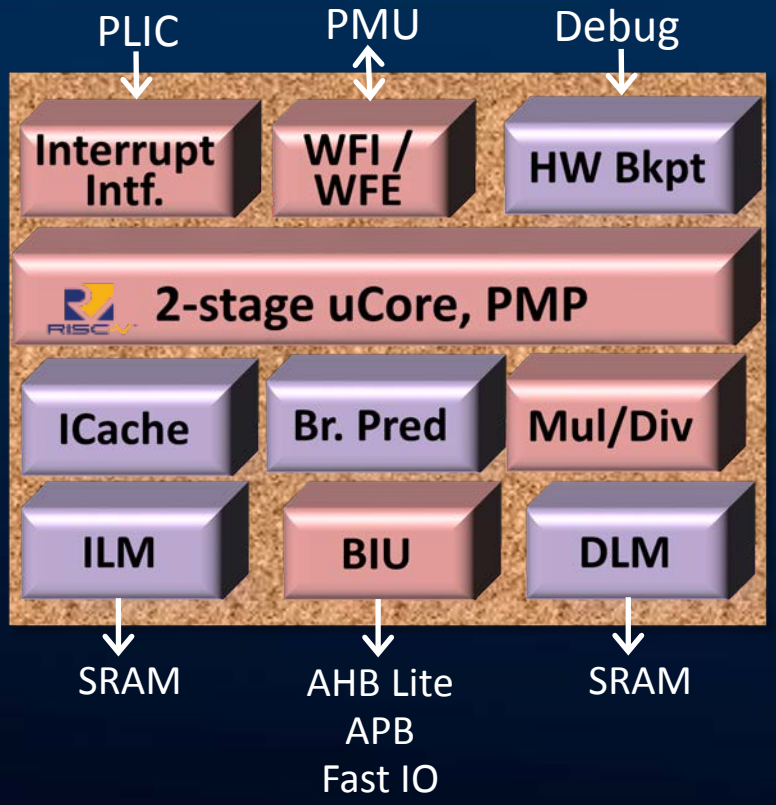
AndesCore™ N22
RISC-V Ultra-Compact Processor

AndesCore™ N22

- **Target applications**
  - Entry level MCU: IoT devices, wearable devices
  - Deeply embedded protocol processing for I/O control, storage, networking, AI and AR/VR
- **Excellent PPA (Power, Performance and Area)**
  - Min. useful configuration: < 15K gates
  - Dynamic power: 1.36 uW/MHz @28nm
  - Performance: 3.95 CoreMark/MHz
  - Max. frequency: up to 700 MHz @worst case
- **Industry quality**
  - Proven in excess of 3.5-billion AndesCore™ SoCs
- **Strong Support Services**

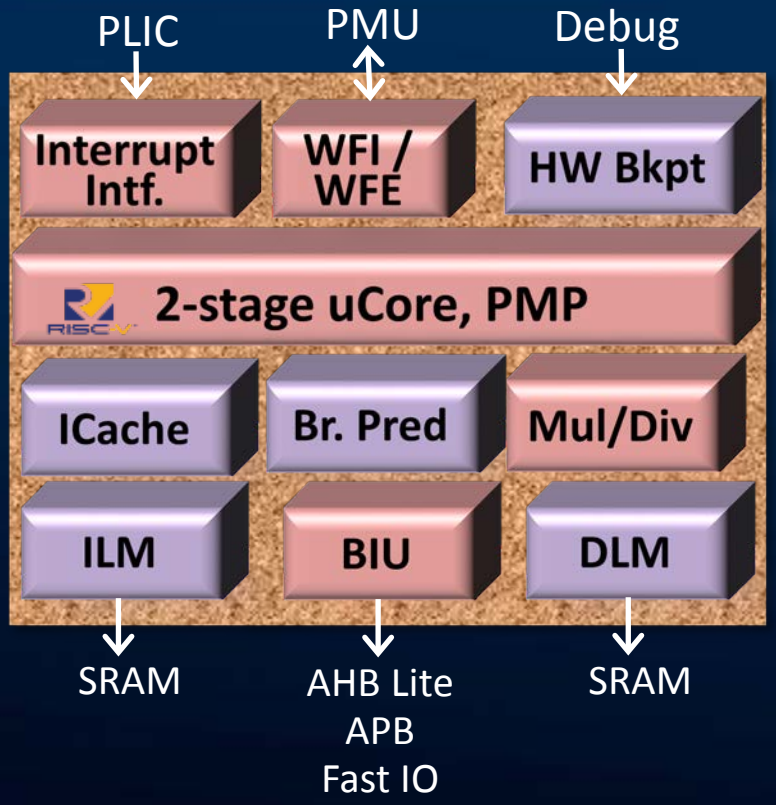
Common Features of N22

- **AndeStar™ V5/V5e ISA (32 bits)**
  - RV32-IMAC, or RV32-EMAC
  - Plus Andes V5 extensions
- **2-stage pipeline, single-issue**
- **Configurable multiplier**
  - Fast (1 cycle) or Small (17 cycles)
- **Optional branch prediction**
  - Static or Dynamic
- **Optional memory subsystem**
  - I/D Local Memory (1KiB to 512MiB)
  - I cache (1KiB to 32KiB; direct-map or 2-way)
  - Misaligned load/store



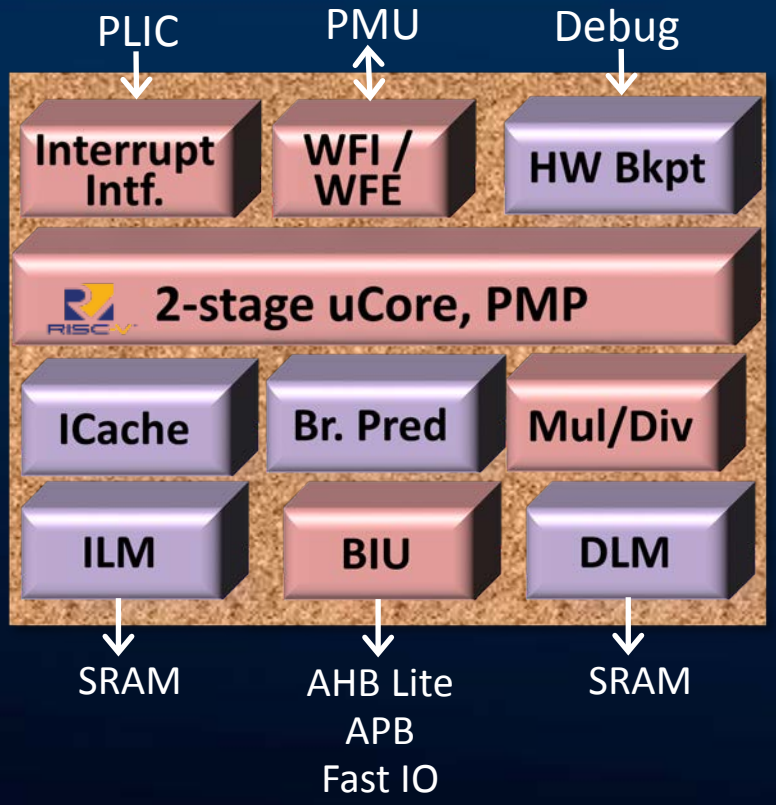
Common Features of N22

- **Physical Memory Protection (PMP)**
  - Up to 16 entries
- **Privilege levels: M-mode**
  - Optional U-mode, for security
- **Power Management:**
  - WFI (wait for interrupt): by WFI instruction
  - WFE (wait for event): through CSR
  - PowerBrake: through CSR
- **Bus interfaces**
  - System Bus Interface: AHB-Lite
  - Optional interfaces:
    - APB for private peripherals
    - Fast I/O interface for single-cycle latency



Common Features of the N22

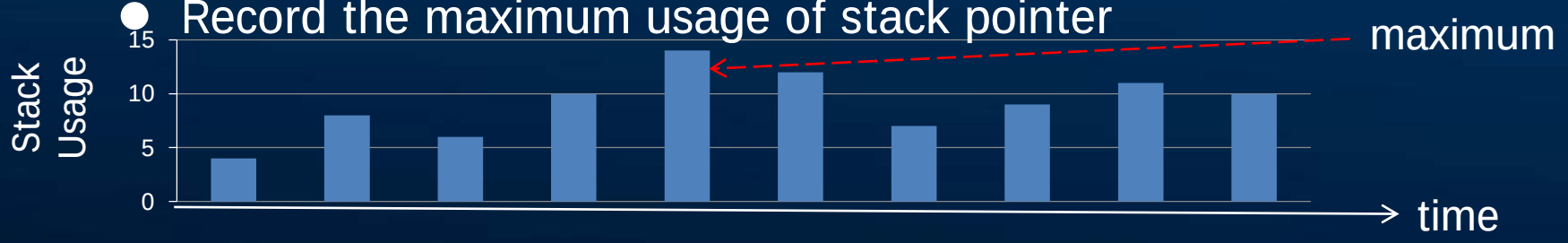
- **Interrupt Controller**
  - Core-Local Interrupt Controller (CLIC)
    - More than 1000 sources, 255 priority levels
    - Selective vectoring with priority preemption
    - Efficient software-based tail chaining
  - Platform-Level Interrupt Controller (PLIC)
    - For multiple cores
    - More than 1000 sources, 255 priorities levels
- **JTAG debug module**
  - up to 8 triggers (breakpoints/watchpoints)
  - 2-wire or 4-wire support



StackSafe™: Protect Stack Usage

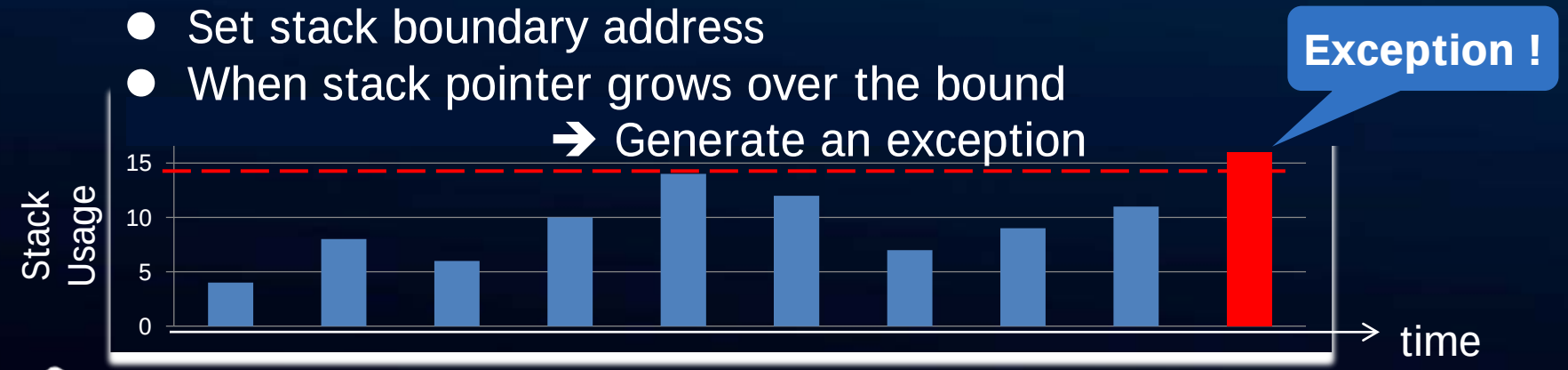
Recording mode:

- Record the maximum usage of stack pointer



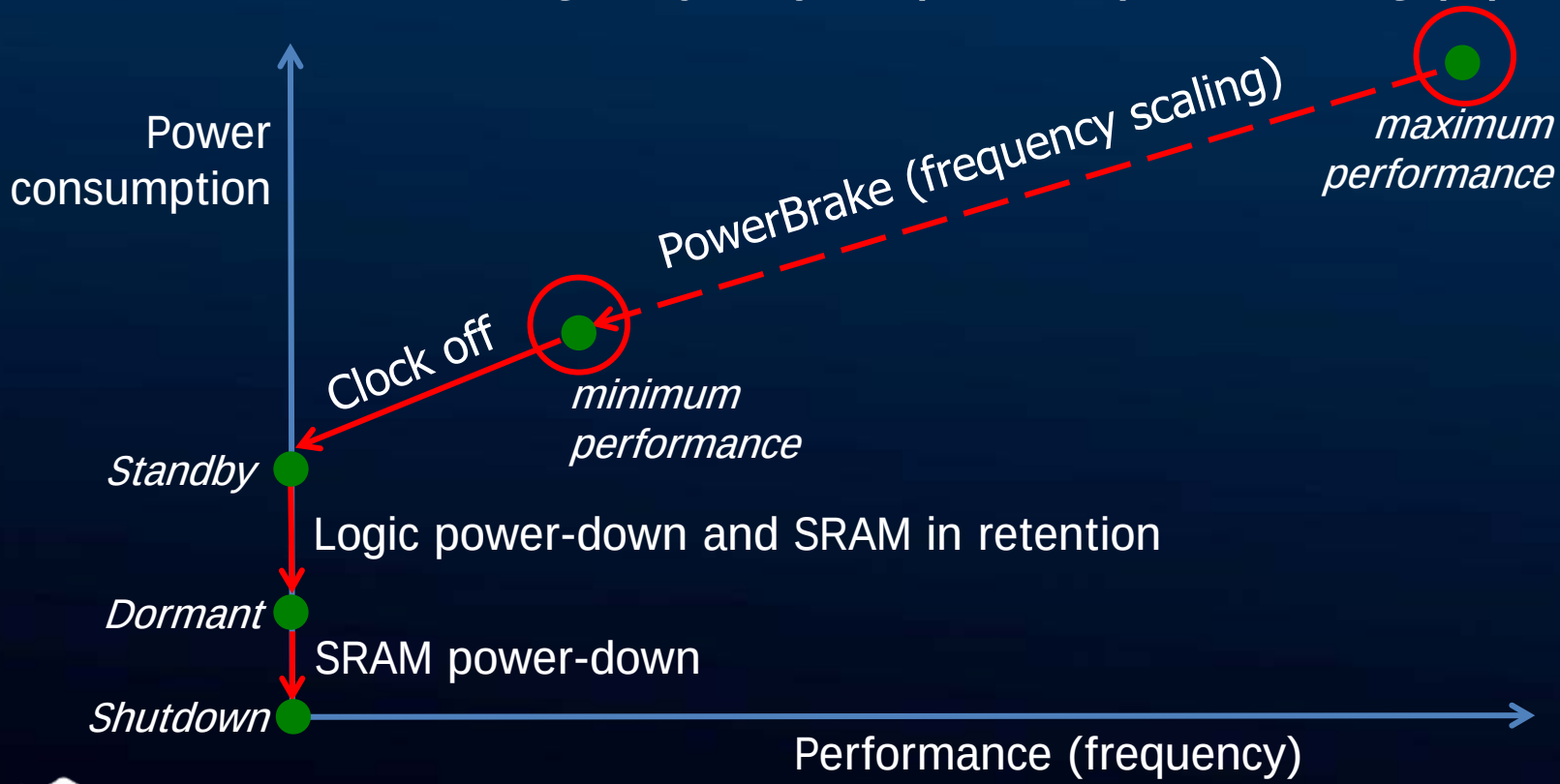
Protection mode:

- Set stack boundary address
- When stack pointer grows over the bound
  - ➔ Generate an exception



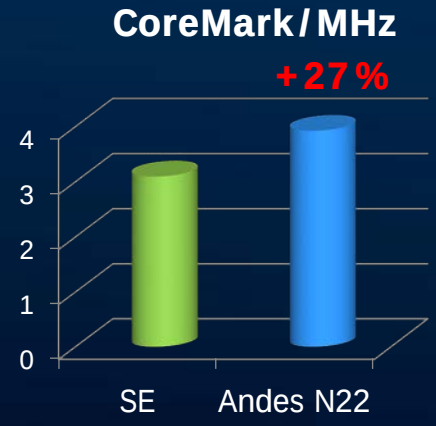
PowerBrake

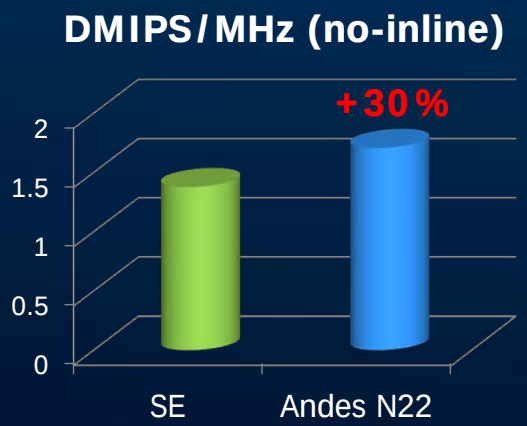
- **PowerBrake** to digitally adjust power (via stalling pipeline)

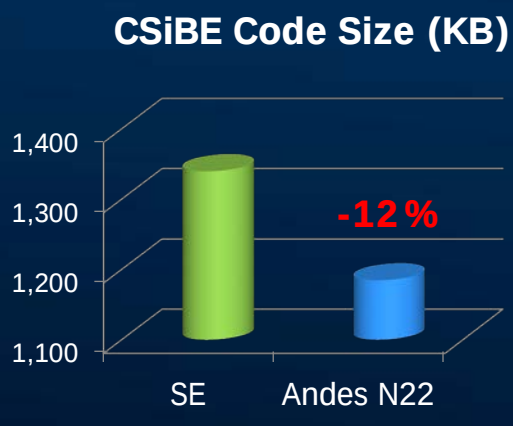


Advantages Over Other RISC-V Cores

- **Higher performance and smaller code size**



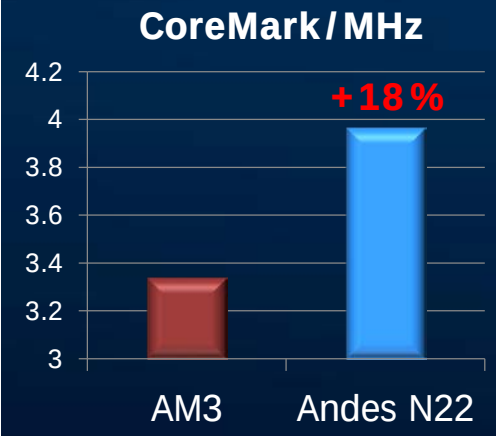


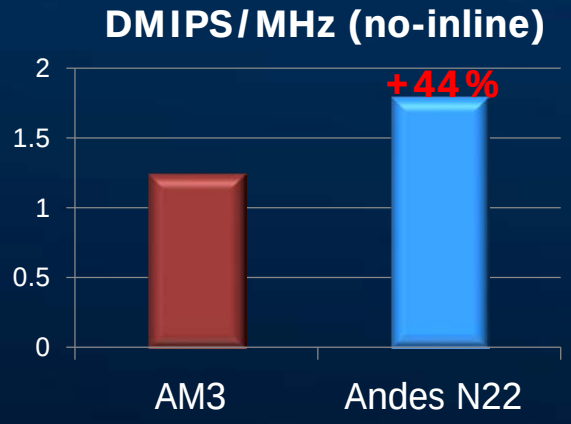


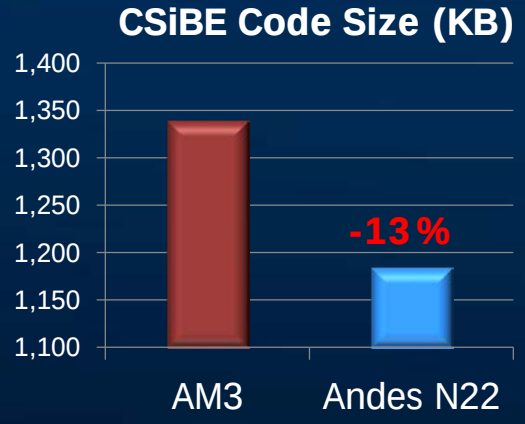
* N22 use the similar configurations as SE

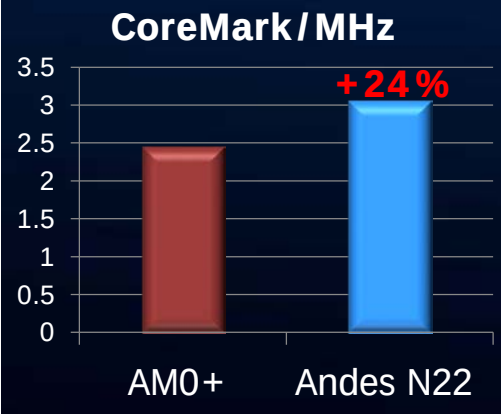
- **Better Verilog RTL code:**
  - CAD-tool friendly and tool-configurable by customers
- **Extended features for embedded applications**
  - Misaligned accesses, StackSafe™, Fast I/O, CoDense™
  - 2-wire debug support to save pin cost

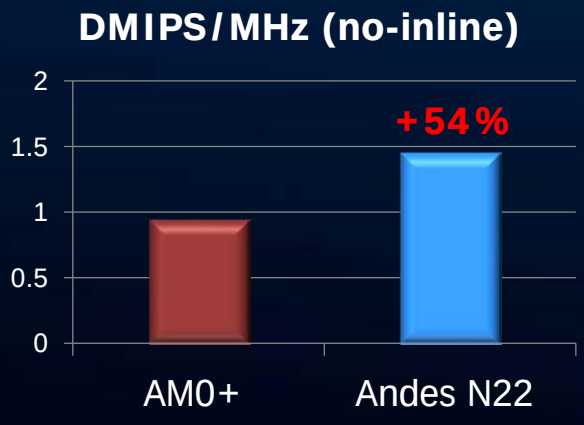
Advantages Over Other Cores











* N22 uses the similar configurations as AM3/AM0+

AndesCore™ N22

BUMBLEBEE

SMALL!

LOW POWER!

LONG ENDURANCE

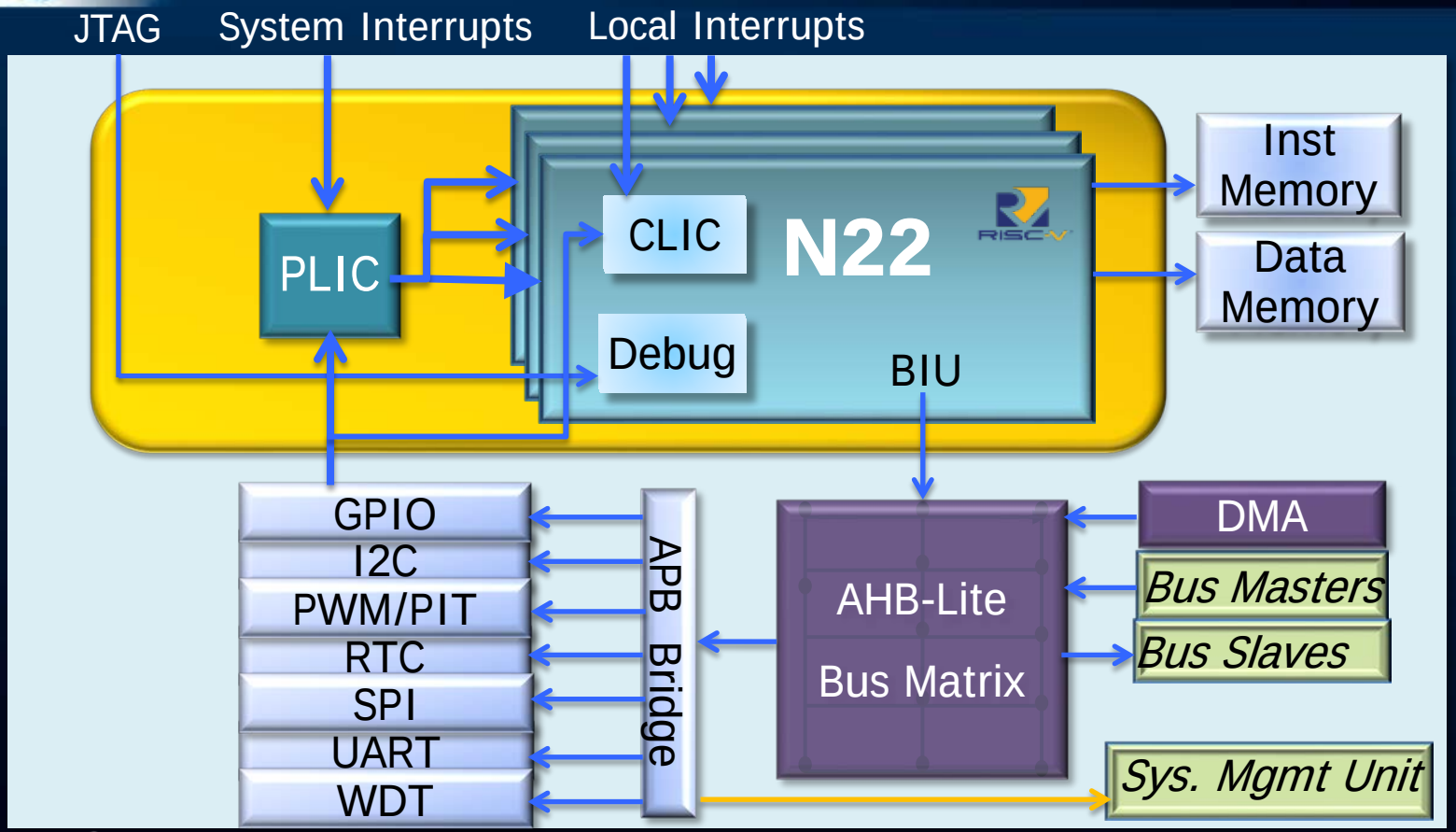
MANY!

PARALLEL

ACCELERATION

Supporting Infrastructure

Pre-integrated Platform for N22



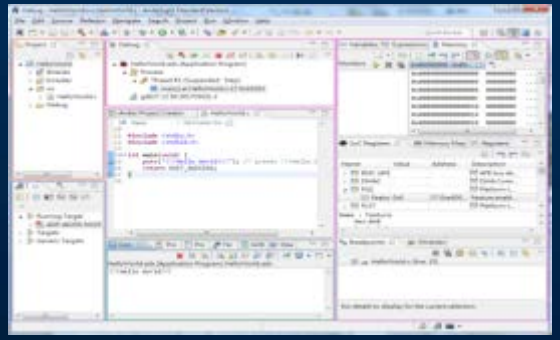
Development Environment

- **AndeSight™ Feature-Rich IDE**
- **AndeSoft™ Software Stack**
- **AndeShape™ Development Boards**
  - Corvette-F1 (Arduino-compatible)
  - ADP-XC7K (Full-Featured)
- **Debugging Hardware**
  - AICE-MINI+, AICE-MICRO
- **Partner Supports**

imperas ultrasoc expresslogic

LAUTERBACH DEVELOPMENT TOOLS SEGGER IAR SYSTEMS *And more …*

AndeSight™ IDE



Corvette-F1

ADP-XC7K

SoC SW Development Environment

AndeSight™ IDE

- Eclipse-Based IDE
- Streamlined GUI
- Feature-rich Editor
- Managed Build System
- Optimized Toolchains
- Source Level Debugger
- Profiling Analysis
- Extensive Demo Projects
- Flash ISP

build executables

debug interactively

AndeSoft™ SW Stack

- Application Layers
- Middleware
- Drivers | App Drivers
- OS/Kernel | Libraries

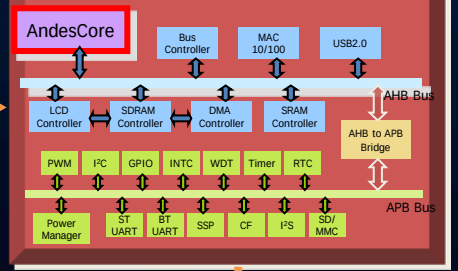
Andes/Partners' Solutions

Customers' Designs

SoC based on AndesCore™

Virtual SoC Configuration

Virtual SoC



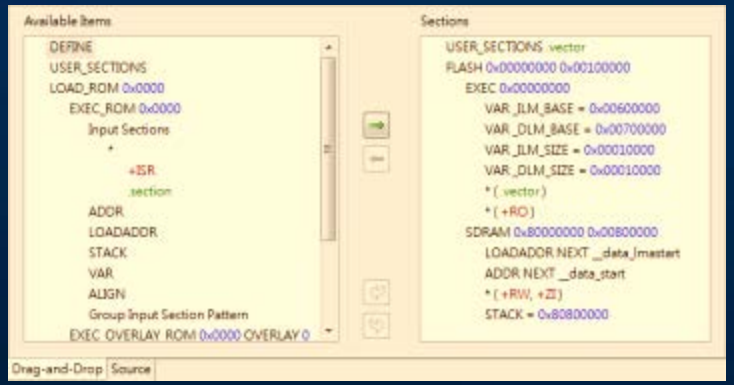
AndeShape™

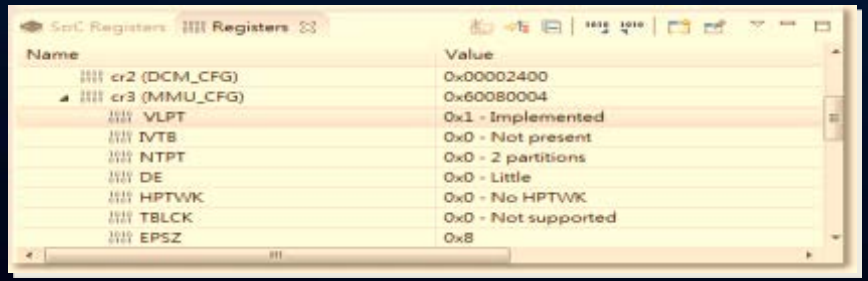
Profiling/Tracing/Debugging data

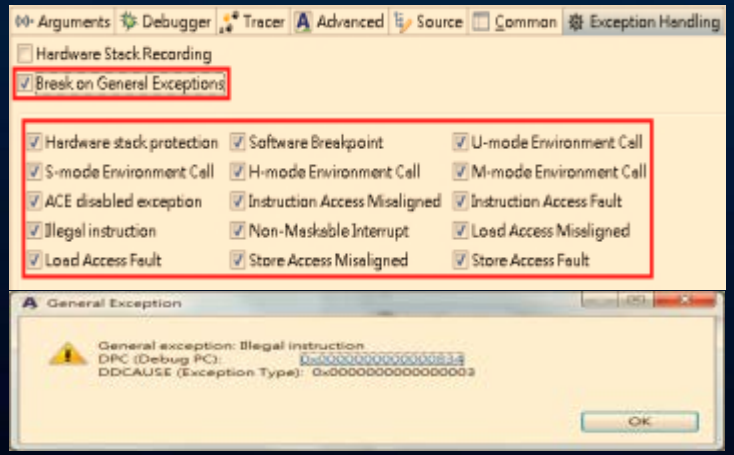
Comprehensive AndeSight™ IDE to Speed Up Software Development

AndeSight™: Professional IDE

- **Eclipse-based**
- **Project Setup:**
  - Meta Linker Script Editor
  - Flash in system programming
- **Debug Support:**
  - Virtual Hosting
  - Register Bit Field Display/Update
  - Break-n-Display on Exceptions

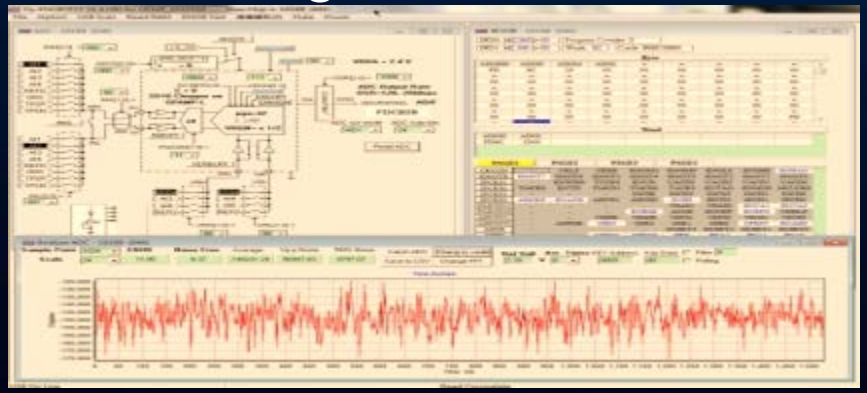


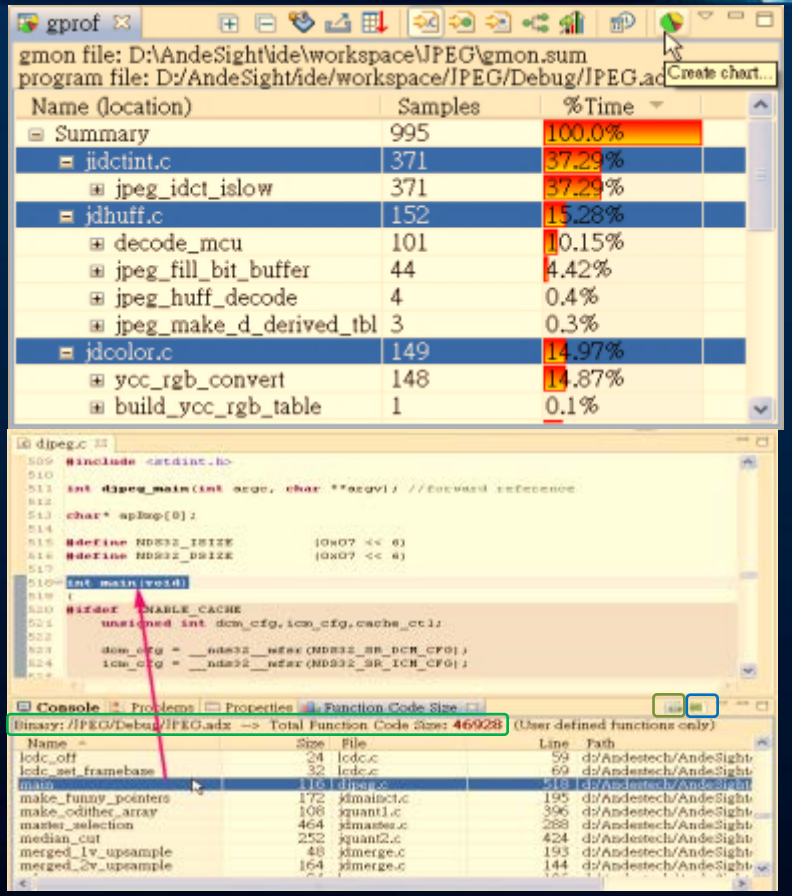




AndeSight™: Professional IDE

- **Program Analysis**
  - Function Profiling
  - Code Coverage
  - Performance Meter
  - Function Code Size
  - (Static) Stack Size
- **Custom Plugin Interface**





Script-Based RTOS Awareness

- Provide RTOS information to help debugging
- Display contents controlled by a Python script

task name	number	priority	start of stack	top of stack	status
"IDLE"	3	0	0x208438 <uxIdleTaskStack.2447>	0x208af0 <...	Running
"Task 2"	2	2	0x200cf8 <ucHeap+2272>	0x2013d0 ...	Delayed
"Task 1"	1	1	0x200430 <ucHeap+24>	0x200b08 ...	Delayed
"Tmr Svc"	4	6	0x208c38 <uxTimerTaskStack.2454>	0x209ac0 <..	Suspended

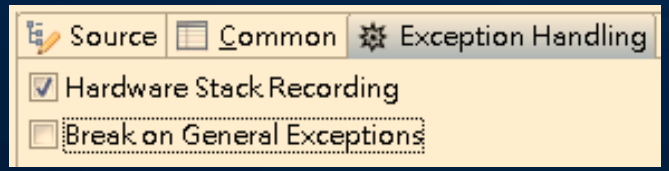
Registers

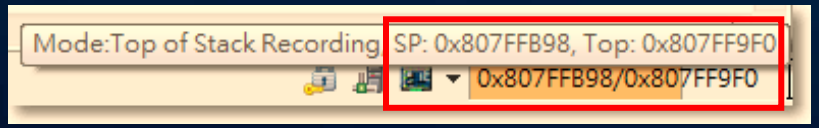
$x1	$x2	$x3	$x4
0x00003d4a	0x002073b0	0x00200900	0x00000000
$x5	$x6	$x7	$x8
0x00000000	0x00000001	0x7ea0c49a	0x0000000a
$x9	$x10	$x11	$x12
0x0020bd08	0x00000000	0x40520000	0x00000000
$x13	$x14	$x15	$x16
0x402b0000	0x80a40000	0x40500000	0x00000000
$x17	$x18	$x19	$x20
0x000007fe	0x0020bcc0	0x7fffffff	0x00000000

queue name	handler address	max length	item size	messages waiting
"TmrQ"	0x200378	5	32	0
task name	number			
"Tmr Svc"	4			

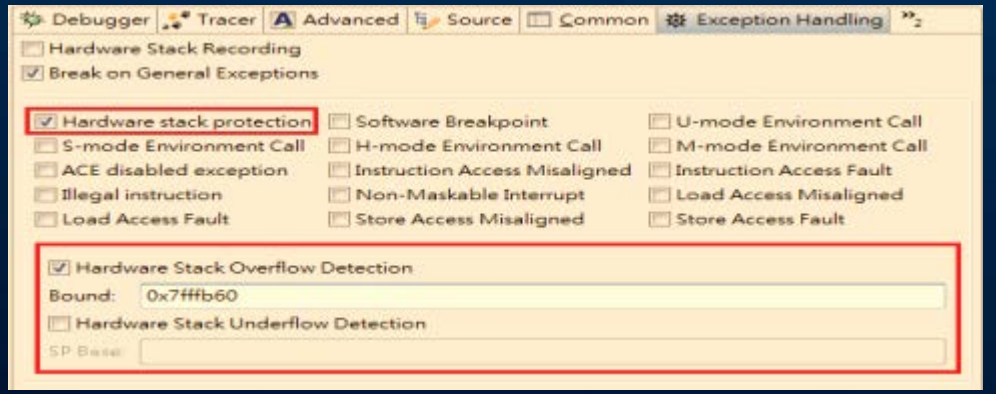
StackSafe™ Protection Handling

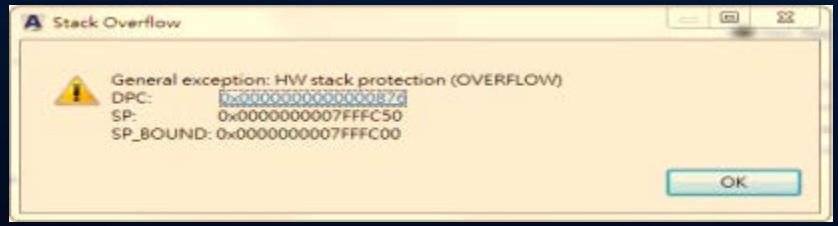
■ Record mode:





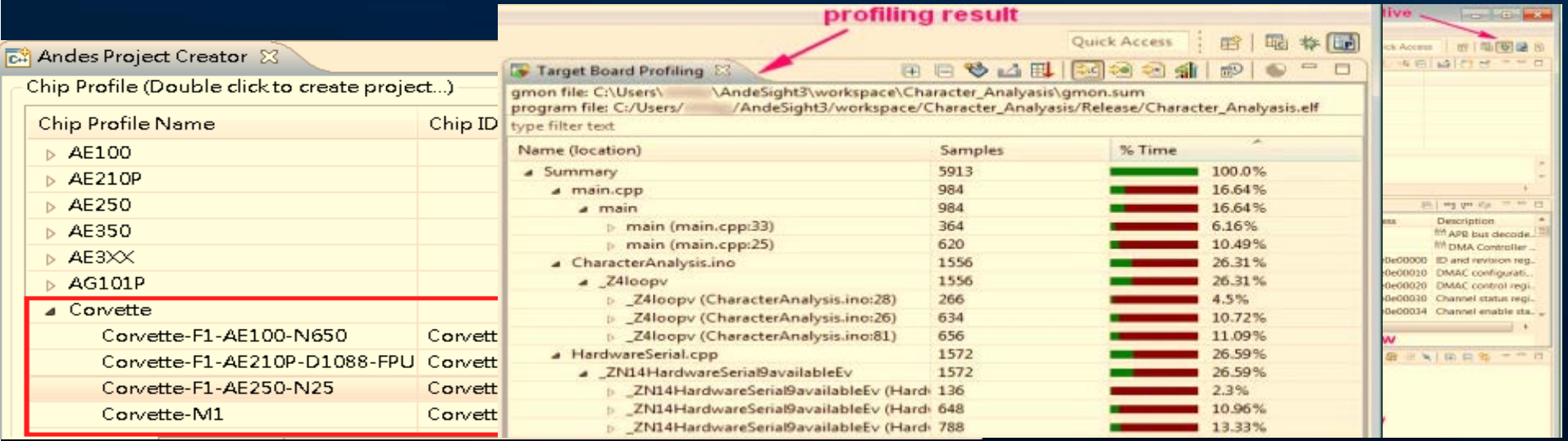
■ Protection mode:





Debug and Analysis for Arduino

- **Official Arduino IDE with limited functions**
  - Not support profiling and debugging (breakpoints/single-stepping)
- **All AndeSight features are available for Arduino development**



AndeSoft™
Application Building Block

AndeSoft™: Application Building Blocks

Fundamental

- Compiler and toolchain are contributed to and supported officially by **GNU and LLVM** communities
- Optimized **MCUlib**, newlib
- Concise linker script and its tool, **Linker Scattering-and-Gathering** (LdSaG)
- **Sample programs** to demo AndesCore™ features

Real-Time Operating Systems

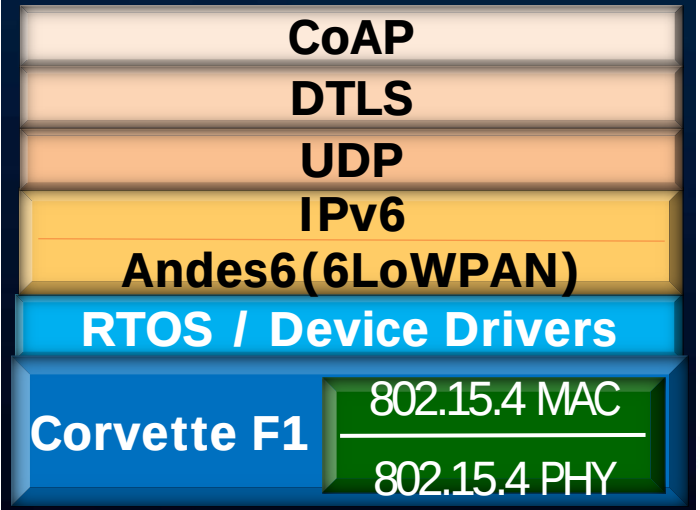
- **FreeRTOS** (open source): 32-bit and 64-bit
- **ThreadX** (from Express Logic): 32-bit and 64-bit
- RISC-V Ready: **Zephyr**, **RT-Thread**, µC/OS-II, MyNewt, SylixOS, LiteOS, AliOS Things

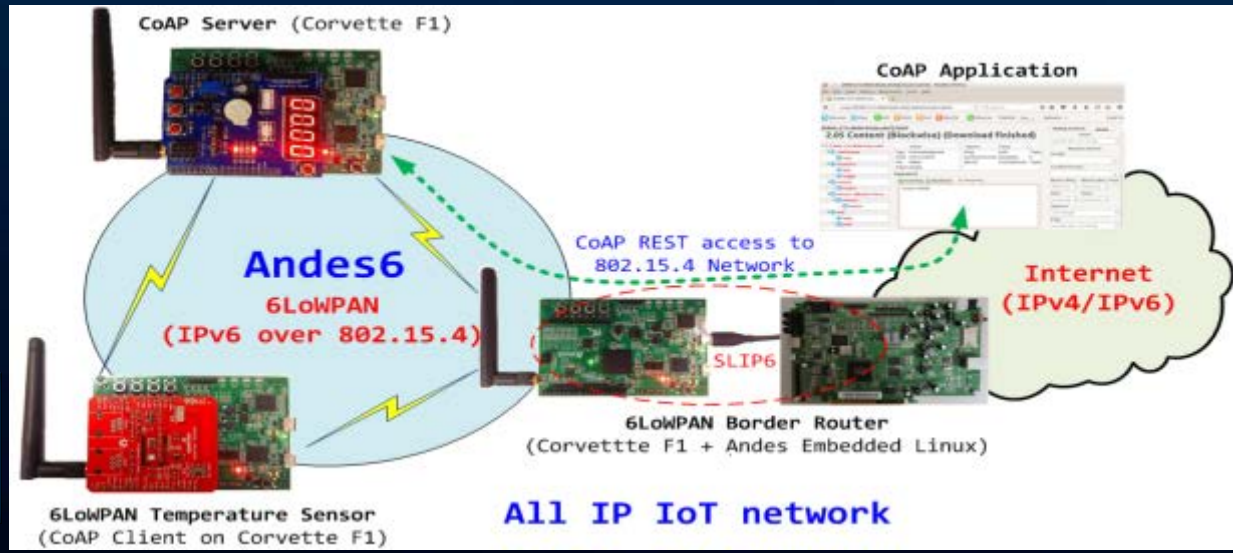
Fundamental Components

- **Commercial-grade Compiler:**
  - **Higher performance and smaller code size**
  - **Comprehensive tool verification**
    - Open source and commercial test suites: >159K test cases
    - Csmith: random C programs generator > 10K test cases per test
    - Support fast-paced continuous advancement for speed optimization and code size
- **Bare metal:**
  - **Rich demo projects for Andes-specific features**
    - PLIC, CLIC, PowerBrake, StackSafe, and more
  - **AMSI (Andes MCU Software Interface) driver APIs**
    - UART, GPIO, RTC, PWM, SPI, I2C and WDT
  - **Easy to use and catch up**

Andes6 (6LoWPAN)

- An implementation of 6LoWPAN (IPv6 over 802.15.4)
- Uses RTOS for OS services
- Either third-party or open source security library can be used for security





Summary

- **AndesCore™ N22**
  - RISC-V Ultra-Compact Processor with excellent PPA
  - Bumblebee: Small! Low Power! Many!

- **Strong supporting infrastructure to achieve fast time-to-market with high quality**
  - Pre-integrated Platform accelerates SoC development
  - AndeSight™ - Rich features speed up SW development
  - AndeSoft™ - Well-integrated building blocks help customers build SoC software quickly and easily

Thank you

AndeSight™ IDE Free Download

- Production-proven AndeSight™ boosts RISC-V development
- A full-featured AndeSight with a three-month time limit
- Download page at http://www.andestech.com/surpport.php?id=4